WHAT IS CLAIMED IS:

1. A semiconductor device manufacturing method comprising:

forming a gate oxide film of a MOS type transistor on a semiconductor substrate;

forming a conductive film that configures a part of a gate electrode on the gate oxide film; and

ion implanting impurities in the semiconductor substrate through the conductive film and gate oxide film.

2. A semiconductor device manufacturing method comprising:

forming a gate oxide film of a MOS type transistor on a semiconductor substrate;

forming a conductive film that configures a part of a gate electrode on the gate oxide film;

removing a part of the gate oxide film and the conductive film formed on a predetermined region of the semiconductor substrate corresponding to an element isolation region forming area;

forming a trench in the semiconductor substrate at the element isolation region forming area from which the part of the gate oxide film and the conductive film are removed;

burying an element isolation oxide layer in the formed trench; and

implanting impurities into the semiconductor

substrate through the conductive film and gate oxide film.

3. A semiconductor device manufacturing method comprising:

forming a gate oxide film of a MOS type transistor on a semiconductor substrate;

forming a first conductive film that configures at least a part of a MOS type transistor gate electrode on said gate oxide film;

forming an etching stopper film having etching selectivity with respect to said semiconductor substrate on said first conductive film;

forming a resist pattern in a region other than a predetermined region for forming an element isolation film on said etching stopper film;

removing said etching stopper film and said first conductive film by using said resist pattern as a mask; and

releasing said resist pattern provided on said etching stopper film, followed by implanting impurities on said semiconductor substrate.

4. A semiconductor device manufacturing method comprising:

forming a gate oxide film of a MOS type transistor on a semiconductor substrate;

forming a first conductive film that configures at least a part of a MOS type transistor gate electrode on

said gate oxide film;

forming an etching stopper film having etching selectivity with respect to said semiconductor substrate on said first conductive film;

forming a resist pattern in a region other than a predetermined region for forming an element isolation film on said etching stopper film;

removing said etching stopper film and said first conductive film by using said resist pattern as a mask;

releasing said resist pattern provided on said etching stopper film;

implanting impurities to a portion on said semiconductor substrate;

forming a trench in said predetermined region for forming an element isolation region of said semiconductor substrate;

burying an oxide layer in said trench and removing said etching stopper film provided on said first conductive film; and

implanting impurities into said semiconductor substrate through said first conductive film and said gate oxide film.

5. A semiconductor device manufacturing method comprising:

forming an oxide film on a semiconductor substrate;

introducing impurities into said semiconductor

substrate through said oxide film;

removing said oxide film, followed by forming a gate oxide film of a MOS type transistor on said semiconductor substrate;

forming a first conductive film that configures at least a part of a MOS type transistor gate electrode on said gate oxide film;

removing said first conductive film and said gate oxide film that exist in a predetermined region for forming an element isolation region, followed by forming a trench on said semiconductor substrate of said predetermined region;

burying an oxide layer in said trench; and

implanting impurities on said semiconductor substrate through said first conductive film and said gate oxide film.

6. A semiconductor device manufacturing method in which a first conductivity type transistor having a first threshold value and a first conductivity type transistor having a second threshold value on a semiconductor substrate, said manufacturing method comprising:

forming an oxide film on said semiconductor substrate;

introducing impurities in a first predetermined region for forming a first conductivity type transistor having a first threshold value and a second

predetermined region for forming a first conductivity type transistor having a second threshold value via said oxide film;

removing said oxide film, followed by forming a gate oxide film of a MOS type transistor on said semiconductor substrate;

forming a first conductive film that configures at least a part of a MOS type transistor gate electrode on said gate oxide film;

removing said first conductive film and said gate oxide film that exist in a predetermined region for forming an element isolation region, followed by forming a trench on said semiconductor substrate of said predetermined region;

burying an oxide layer in said trench;

forming a resist pattern that covers the first conductivity type transistor region having at least the second threshold value; and

implanting impurities into said semiconductor substrate through said gate oxide film in a predetermined region for forming the first conductivity type transistor having the first threshold value using said resist pattern as a mask.

7. A semiconductor device manufacturing method in which a plurality of identical conductivity type transistors having gate oxide films with different film thickness on a semiconductor substrate, said

manufacturing method comprising:

forming a first gate oxide film on said semiconductor substrate;

forming a second gate oxide film having a film thickness different from that of the first gate oxide film;

forming a first conductive film on said first gate oxide film and second gate oxide film;

removing said first conductive film and said first gate oxide film that exist in a predetermined region for forming an element isolation region and a second gate oxide film, followed by forming a trench on said semiconductor substrate of said predetermined region;

burying an oxide layer in said trench; and

implanting impurities into said semiconductor substrate through said first conductive film, said first gate oxide film, and said second gate oxide film at the same time.

8. A semiconductor device manufacturing method according to any one of claims 1 to 7, wherein said first conductive film is a polycrystalline silicon film.

9. A semiconductor device manufacturing method according to claim 8, wherein said first conductive film is a polycrystalline silicon film of 300 nm or less in thickness.

10. A semiconductor device manufacturing method

according to claim 9, wherein a second conductive film is laminated on said first conductive film.

11. A nonvolatile memory device manufacturing method having a multi-layered gate electrode type transistor provided on a semiconductor substrate, said manufacturing method comprising:

forming a gate oxide film of a MOS type transistor on a semiconductor substrate;

forming a first conductive film that configures at least a first layer of a multi-layered gate electrode of the MOS type transistor on said gate oxide film;

removing a portion of said first conductive film and said gate oxide film that corresponds to a predetermined region for forming an element isolation region, followed by forming a trench in said semiconductor substrate corresponding to said predetermined region for forming the element isolation region;

burying an oxide layer in said trench;

implanting impurities into said semiconductor substrate through said first conductive film and said gate oxide film; and

forming a second conductive film that configures a second layer on said first conductive film via an insulation layer to form a multi-layered gate electrode.

12. A semiconductor device manufacturing method according to claim 11, wherein said first conductive

film has at least a two-layered polysilicon laminate structure.

13. A nonvolatile memory device manufacturing method having a multi-layered gate electrode type transistor provided on a semiconductor substrate, said manufacturing method comprising:

forming a gate oxide film of a MOS type transistor on the semiconductor substrate;

forming a first conductive film that configures at least a first layer of a multi-layered gate electrode of the MOS type transistor on said gate oxide film;

forming an etching stopper film having etching selectivity with respect to the semiconductor substrate on said first conductive film;

forming a resist pattern in a region other than a portion that corresponds to an element isolation forming region on said etching stopper film;

removing said etching stopper film and said first conductive film using said resist pattern as a mask;

releasing said resist pattern provided on said etching stopper film, followed by implanting impurities on said semiconductor substrate; and

forming a second conductive film on said first conductive film via an insulation layer to form a multi-layered gate electrode.

14. A nonvolatile memory device manufacturing method having a multi-layered gate electrode type

transistor provided on a semiconductor substrate, said manufacturing method comprising:

forming a gate oxide film of a MOS type transistor on said semiconductor substrate;

forming a first conductive film that configures at least a first layer of a multi-layered gate electrode of the MOS type transistor on said gate oxide film;

forming an etching stopper film having etching selectivity with respect to said semiconductor substrate on said first conductive film;

forming a resist pattern in a region other than a portion that corresponds to an element isolation forming region on said etching stopper film;

removing said etching stopper film and said first conductive film using said resist pattern as a mask;

releasing said resist pattern provided on said etching stopper film, followed by implanting impurities on said semiconductor substrate via said gate oxide film; and

forming a second conductive film on said first conductive film via an insulation layer to form a multi-layered gate electrode.

15. A nonvolatile memory device manufacturing method having a multi-layered gate electrode type transistor provided on a semiconductor substrate, said manufacturing method comprising:

forming a gate oxide film of a MOS type transistor

on said semiconductor substrate;

forming a first conductive film that configures at least a first layer of a multi-layered gate electrode of the MOS type transistor on said gate oxide film;

forming an etching stopper film having etching selectivity with respect to said semiconductor substrate on said first conductive film;

forming a resist pattern in a region other than a portion that corresponds to an element isolation forming region on said etching stopper film;

removing said etching stopper film and said first conductive film using said resist pattern as a mask;

releasing said resist pattern provided on said etching stopper film, followed by implanting impurities on said semiconductor substrate;

forming a trench in said semiconductor substrate corresponding to said element isolation forming region;

removing said etching stopper film provided on said first conductive film at the same time when an oxide layer is buried in said trench;

implanting impurities into said semiconductor substrate through said first conductive film and said gate oxide film; and

forming a second conductive film on said first conductive film via an insulation layer to form a multi-layered gate electrode.

16. A semiconductor device manufacturing method in

which a first transistor of a first conductivity type having a first threshold value and a second transistor of a first conductivity type having a second threshold value are formed in a peripheral circuit together with a nonvolatile memory device in which a multi-layered gate electrode type transistor is formed as a memory cell on a semiconductor substrate, said manufacturing method comprising:

forming an oxide film on a semiconductor substrate;

introducing impurities into a first region for forming a first transistor of a first conductivity type having a first threshold value and a second region for forming a second transistor of a first conductivity type having a second threshold value via said oxide film;

removing said oxide film, followed by forming a gate oxide film that configures a MOS type transistor on said semiconductor substrate;

forming a first conductive film that configures at least a first layer of a MOS type transistor gate electrode on said gate oxide film;

removing a portion of said first conductive film and said gate oxide film that corresponds to an element isolation region, followed by forming a trench in said semiconductor substrate for forming the element isolation region;

burying an oxide layer in said trench;

forming a resist pattern that covers at least the second region of the first conductivity type transistor having the second threshold value;

implanting impurities into said semiconductor substrate through said gate oxide film in the first region of the first conductivity type transistor having the first threshold value using said resist pattern as a mask; and

forming a second conductive film on said first conductive film via an insulation layer to form a multi-layered gate electrode.

17. A method for manufacturing a semiconductor device having a peripheral circuit composed of a plurality of transistors of the same conductivity type and an nonvolatile memory device with a multi-layered gate electrode type transistors as memory cells on a semiconductor substrate, wherein the plurality of transistors that configures the peripheral circuit have gate oxide films with different film thickness, the semiconductor device manufacturing method comprising:

forming a first gate oxide film on the semiconductor substrate;

forming a second gate oxide film with its film thickness different from that of said first gate oxide film;

forming a first conductive film on said first gate

oxide film and said gate oxide film;

removing a portion in the first conductive film, first gate oxide film, and second gate oxide film corresponding to a predetermined region for forming an element isolation film, followed by forming a trench in said semiconductor substrate at said predetermined region for forming the element isolation film;

burying an oxide layer in said trench;

implanting impurities into said semiconductor substrate via said first conductive film, first gate oxide film, and second gate oxide film at the same time; and

forming a second conductive film on said first conductive film via an insulation layer to form a multi-layered gate electrode.